NABU Commercial Terminals Ltd.

NABU 3100 Service Manual

PRELIMINARY

August 3, 1983

PREFACE

The NABU 3100 Service Manual was developed as a complete instruction manual for the NABU 3100 Video Display Terminal. Although the technical description and operation is detailed, it is assumed that only trained and qualified service technicians will attempt to disassemble or repair the units. NABU Manufacturing Corporation has prepared a course of instruction to inform suitable service technicians on repair techniques for the NABU 3100 Video Display Terminal.

The NABU 3100 Video Display Terminal (NABU 3100) is constructed to strict safety standards, but very high voltages are generated within the display unit, which could be a hazard to life; therefore, great care should be exercised when removing the covers of the NABU 3100. Covers should only be removed when the supply cord is disconnected.

The NABU 3100 Service Manual is organized in a logical fashion, using the following format:

Chapter 1

Introduction - A general introduction to the manual, its scope and purpose. The physical and functional characteristics are also included in this chapter.

Chapter 2

Description and Operation - A technical description and operation of the NABU 3100, in a modular manner. Each module is described in its relative position of importance within the terminal.

Chapter 3

Testing And Troubleshooting - A logical approach to defining and identifying a fault or malfunction within the NABU 3100.

Chapter 4

Disassembly And Repair - The correct methods of disassembling and assembling the modules of the NABU 3100.

Chapter 5

Alignments - The alignment procedures, presented in a logical sequence, that must be carried out after replacement of defective modules or components.

Chapter 6

Illustrated Parts List - The identification and location of components and modules that field service personnel are authorized to replace.

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CHAPTER ONE

INTRODUCTION

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1.1 INTRODUCTION

The NABU 3100 Video Display Terminal (NABU 3100), shown in Figure 1.1, is a smart data terminal based on the logic of a Z-80 microprocessor. The NABU 3100 is capable of communicating with a host computer, in either a full-duplex or half-duplex mode, through an interface cable operating under the RS-232C standard rules.

The standard features of the NABU 3100 are as follows:

- Keyboard - Detached, with a coiled cable connection to the terminal. Full typewriter layout, with separate 14-key numeric pad plus cursor control keys.
- Display - 24 lines x 80 columns (one page) of characters.
- Status line - 25th line (beneath the page), user-selectable, user-writeable.
- Display background - Grey, or optional purchase (green or amber).
- Split screen - User-definable, split size.
- Display memory - 1 page (second page optional purchase).
- Scrolling - Keyboard-selectable, smooth or jump scroll.
- Display characters - 7 x 9 dot matrix in a 9 x 10 dot field; may be double width on a single line. Four different highlights on a character are possible: blink, bold, reverse, and with underscore.
- Editing - Full editing functions, with protected fields.
- User strings - 16 user-programmable strings on 8 keys.
- Escape sequences - ANSI X 3.64-compatible.
- Transmission - Block transmission capability: line, page and/or partial page.

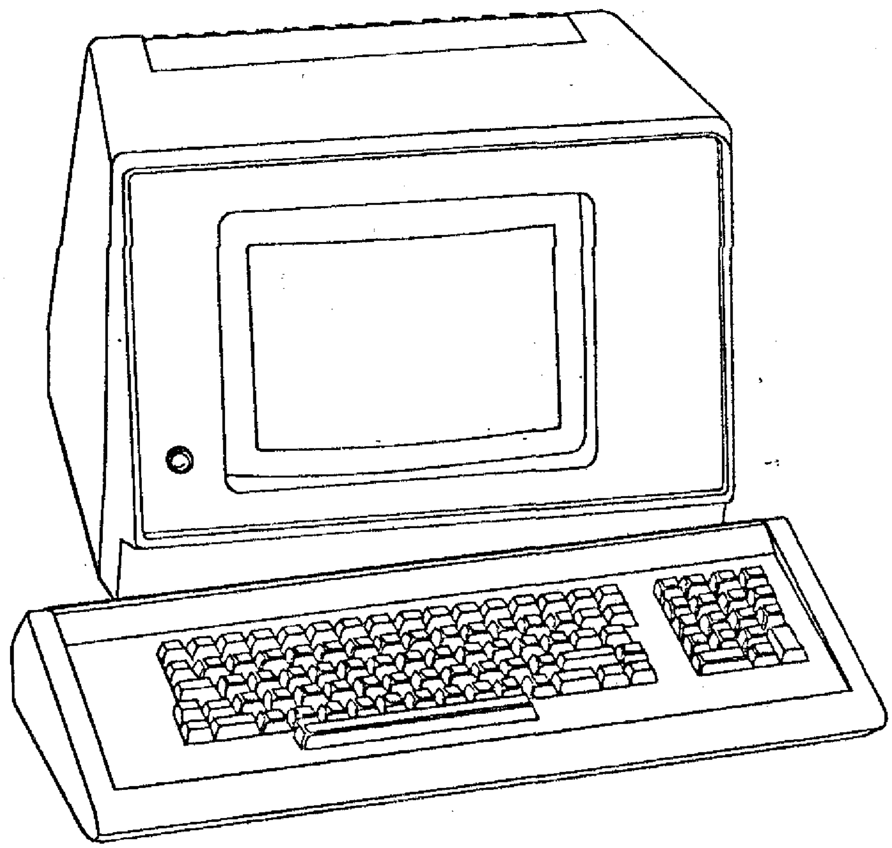


Figure 1.1 NABU 3100 Video Display Terminal

- Data transmission speeds - 15 baud rates from 50 up to 9,600. Transmit and receive speeds are independantly selectable.

- Power Requirements - nominal 110 or 220 VAC, 60 or 50 Hz, depending on the model.

Optional features that may be purchased are:

- Composite video output.
- Background: green or amber.
- Display memory: second page.
- National character sets.
- Output: bi-directional, buffered serial-peripheral port.

1.2 PHYSICAL CHARACTERISTICS

The NABU 3100 Video Display Terminal has the physical characteristics shown in Table 1.1.

NAME	CHARACTERISTICS
Available versions:	
Standard	With keyboard.
Receive Only	Without keyboard.
Dimensions	W D H
Standard (c/w keyboard)	51.5 cm x 55.5 cm x 34.0 cm.
Display Only	42.0 cm x 37.5 cm x 34.0 cm.
Keyboard	51.5 cm x 22.5 cm x 8.5 cm.
Weight	
Standard	16.5 kg.
Display	13.3 kg.
Keyboard	3.2 kg.
External Connections	
Display	J1 - AC power input. J2 - Keyboard connector. J3 - Optional serial data communications interface. J4 - Serial data communications interface to modem or host computer.
Keyboard	J1 - Connector to display.
Configuration	NABU 3100 115v, 50/60 Hz. NABU 3100/EXP 230v, 50/60 Hz.
Power Consumption	
NABU 3100	150/130 VAC, 50/60 Hz.
NABU 3100/EXP	210/260 VAC, 50/60 Hz.

Table 1.1 **Physical Characteristics of the NABU 3100**

NAME	CHARACTERISTICS
Overload Protection NABU 3100	Fused 1A Fast Blow.
NABU 3100/EXP	Fused Dual 0.6A Fast Blow.

Table 1.1 **Physical Characteristics of the NABU 3100 (Continued)**

1.3 INTERFACE CHARACTERISTICS

The interface characteristics of the NABU 3100 are as shown in Table 1.2.

NAME	CHARACTERISTIC
Interface Cables J2 terminal to keyboard	Conforms to Standard RS-232C (CCITT-V.24).
Current-Loop Adaptor Cable	Special, 20 mA consumption.
J3 to peripherals	Conforms to Standard RS-423.
J4 to host computer	Conforms to Standard RS-423.
Communication from J4	
Code	ASCII and ANSI x 3.64-compatible Escape Sequences.
Type	Serial Asynchronous, switchable XON, XOFF or DTR control from local or host computer.
Speed	50 to 19200 baud, split send/receive.
Method	Sequential character in Conversational mode, or by line, message, or page in Buffered Transmit mode.
Mode	Full-Duplex, Half-Duplex or Echoplex.
Character length	7- or 8-bit, selectable.
Parity	Odd/Even/None, selectable.

Table 1.2 **Characteristics Of NABU 3100 Interfaces**

CHAPTER TWO

CIRCUIT DESCRIPTION

CHAPTER TWO - CIRCUIT DESCRIPTION

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2.1 INTRODUCTION

The NABU 3100 is a direct entry terminal able to transmit and recieve data from a host computer, one character at a time, or send to a host computer from the keyboard. The keyboard translates an input from the key matrix (key pressed) into a coded binary character compatible with the ASCII code. This character is written into the memory of the host computer together with any command bytes which may be necessary for special attributes of the character. The host computer responds by transmitting the characters back to the terminal. The terminal inspects the command bytes and directs the character to the screen character memory, and directs the commands to the attribute memory to determine the visual appearance of the character.

The screen scan rate is 10 scan lines per character height, and to ensure that only complete characters are displayed on the screen, the scan lines are joined by a link list method of accessing memory. The list contains the count for the scan lines and resets on the 10th line, preventing interrupts from stopping the character scan.

There are three memories built into the NABU 3100, one is a read only memory where the operating program is permanently stored, another for the attribute information, and finally one for a scratch pad memory where incoming data is stored.

2.2 CONTROLLER

The NABU 3100 users a Z-80 microprocessor and its associated program memory to control the functions of the unit at a rate determined by a crystal controlled oscillator operating at 14.7456 MHz. The controller contains all of the controlling circuits including the microprocessor and is mounted on a single printed circuit board (PCB). The circuits use integrated circuits to perform the following functions:

a. Central Processing Unit (CPU) to control the functions of the NABU 3100. The CPU schedules information and determines the routing of information.

b. Timer to generate master timing signals to gate information between the various blocks of the NABU 3100. The timer and the CPU derive their timing cycle from the 14.7456 MHz crystal oscillator. All timing functions are multiples of this frequency and asynchronous signals from the NABU 3100 input ports are translated to conform to this timing cycle.

c. Program Memory contains the operating program of the NABU 3100 it is a read only memory and is accessed by the CPU to perform the functions required.

d. Scratch pad Memory is a read-write memory used as a data storage medium for data to and from the host computer.

e. Character memory is a read-write memory used to store screen character data.

f. Attribute memory is a read-write memory used to store attribute data. The major attributes use in the 3100 are double width characters and character highlighting.

g. Screen character data drivers copies the output of the character memory onto a line buffer for transmission to the Cathode Ray Tube (CRT). These drivers are actuated during a CRT copy cycle.

h. Universal Asynchoronous Receiver Transmitters (UART's) match the CPU transmission rate to the keyboard and the input ports transmission rates. The UART's generate the correct signal timing rates.

i. The controller incorporates a set of option switches and their associated drivers to select the options available to the NABU 3100. The major options are, change of baud rate, data coding and national character sets.

The controller interfaces with video circuits to produce and refresh the characters on the CRT display. The video circuits are contained on a separate PCB called the Monitor.

The controller uses buses to interconnect the functional units of the system, there are four major buses, the address bus, the data bus, the control pulse bus, and the chip select bus.

2.2.1 Address Bus

The address bus is a 16-bit address bus (A0 to A15) connecting the functional modules of the NABU 3100 illustrated in figure 2.1. When the CPU requires data it sends an address through the address bus to identify the location of the data required by the operating program.

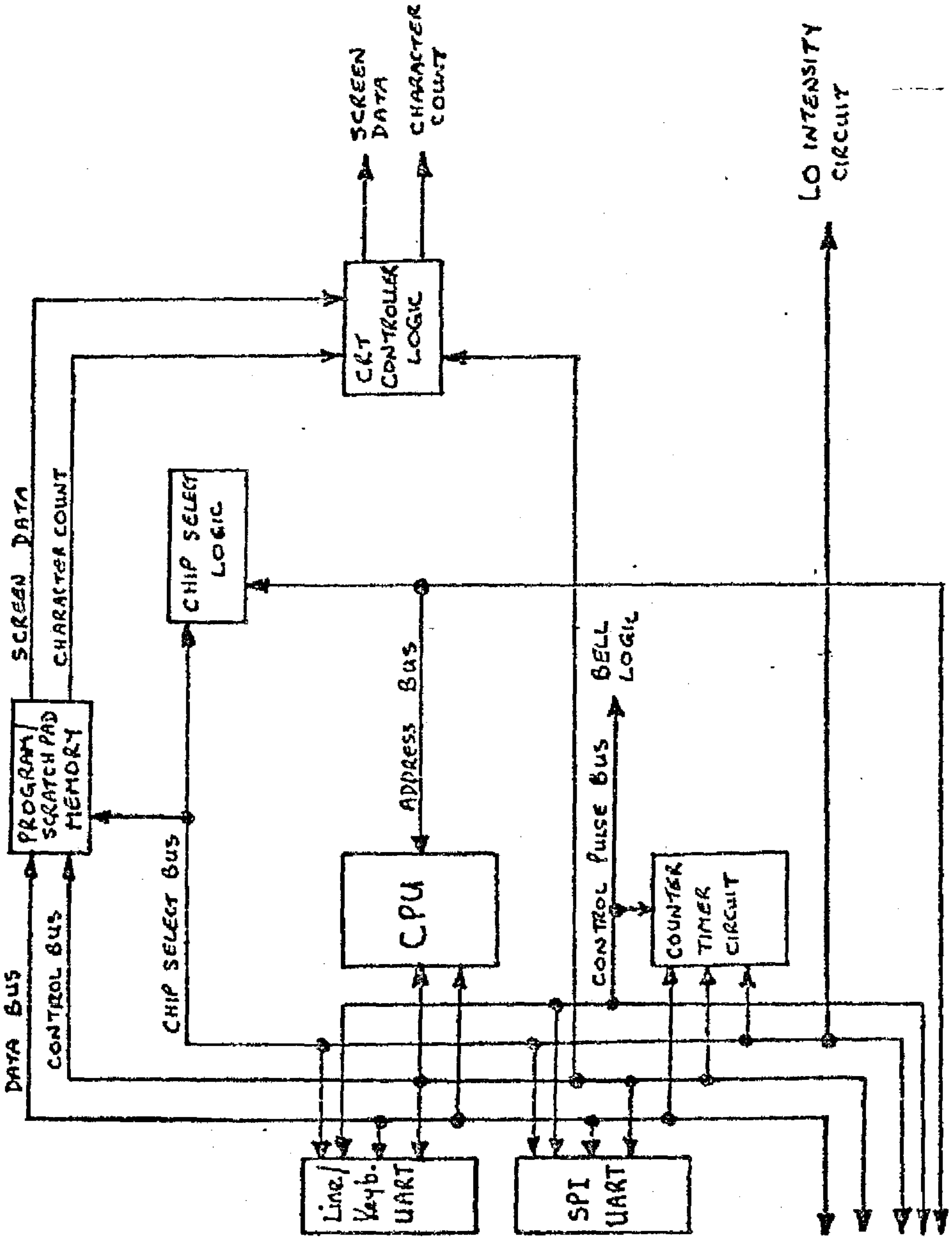


Figure 2.1 Bus Interconnection Diagram

The address bus accesses the following modules which are also illustrated in a block diagram form in figure 2.2:

a. The four EPROM (External Programmable Read Only Memory) memories which form the Program Memory. The EPROM's form a 16K x 8 bit read only memory located at positions 16D, 17D, 19d and 20D on the controller PCB.

b. The two memory modules forming the Scratch Pad Memory. The memory is a 1K x 8bit read-write memory located at positions 11B and 16B on the controller PCB.

c. The eight Random Access Memory (RAM) modules forming the Character Memory. The memory is a 4K x 8 bit read-write memory located at positions 12B, 13B, 14B, 15B, 17B, 18B, 19B, and 20B on the controller PCB.

d. The four RAM modules forming the Attribute Memory. The memory is a 4K x 4 bit read-write memory located at positions 17B, 18B, 19A,and 20A on the controller PCB.

e. The two decoders forming the memory chip select (CS) signal decoders. The decoders generate the select signals for the appropriate memory. The decoders are located at 17F and 19F on the controller PCB.

f. A Buffer module to increae the drive capability of the screen address lines A0-A3, and A5. The Buffer module is located at 16F on the controller PCB.

g. Three Driver modules to drive the screen address lines during the period of time the CRT Controller is copying data from the screen memory to the line buffer memory. The Driver modules are located at 12D, 13D, and 15D on the controller PCB.

2.2.2 Data Bus

The data bus is connected to the input/output connections of the addressable memories described in 2.2 and illustrated in figure 2.1 Data is channelled through the data bus to form the characters displayed on the CRT screen. A link list method of access to data ensures that a character scan is completed before accessing a new character line. A block diagram of the data bus is shown in figure 2.3 and 2.4, the data bus is directly connected to the screen data bus.

The data bus also has access to the following controlling circuits:

a. Two driver modules used to copy the output of the screen character memory into the line buffer memory during a CRT copy cycle. The driver modules are located at 10A and 11A on the controller PCB.

b. A Driver module used to copy the output of screen data memory into the line buffer memory during a CRT copy cycle. The driver module is located a 10B on the controller PCB.

c. A dual UART module connecting the CPU to the line and to the keyboard. The UART module is located at 7F on the controller PCB.

e. A programmer timer module used to generate three UART clock pulses and one software timing function to control the operation of the various UART's in the controller. The programmer timer module is located at 4G on the controller PCB.

f. A driver module to read the settings on the option switches. The driver module is located at 21H on the controller module.

2.2.3 Control Pulse Bus

The control pulse (CP) bus is the highway used by the control signals generated by various functional circuits of the NABU 3100. The control signals have mnemonic names generally derived from a description of the signal function. The major signals using the CP bus are shown in figures 2.5, 2.6, and 2,7.

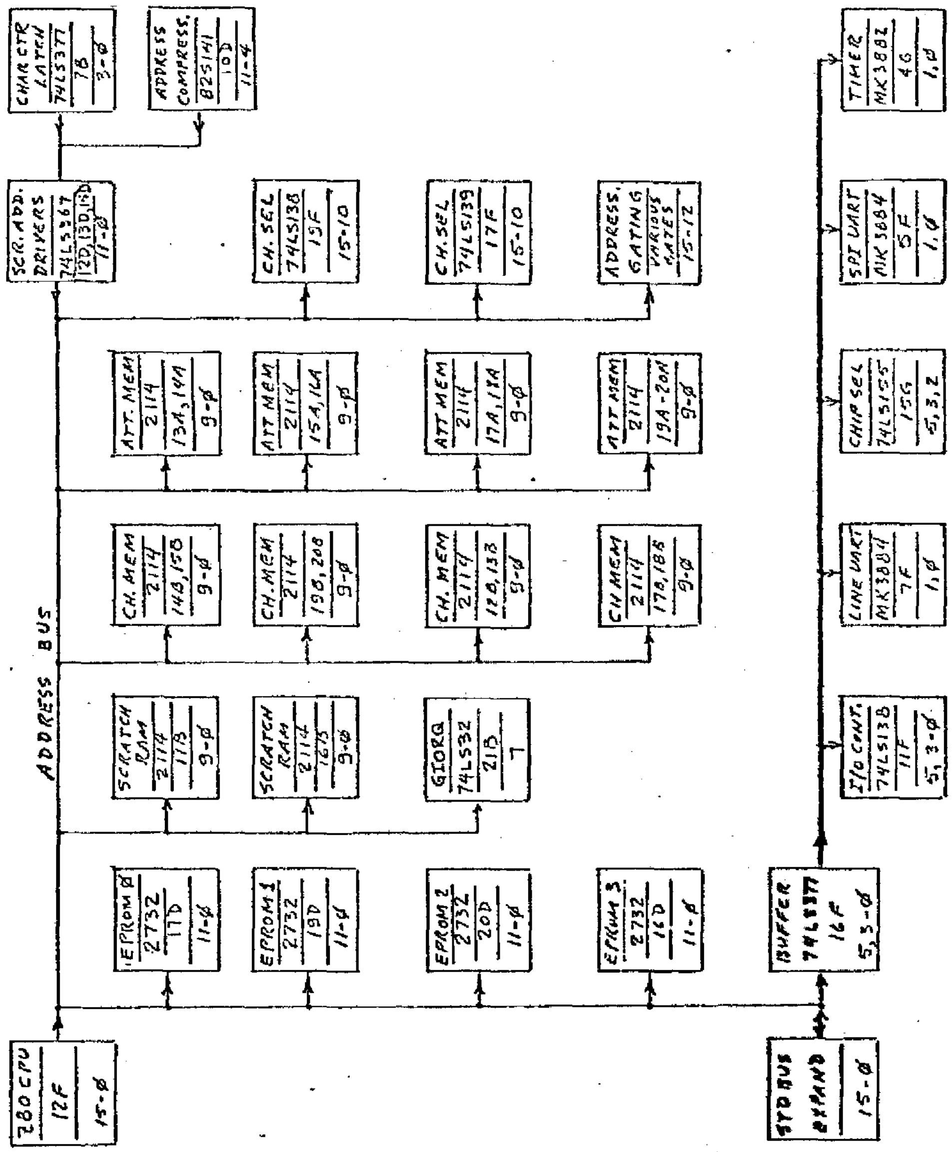


Figure 2.2 Block Diagram of the Address Bus

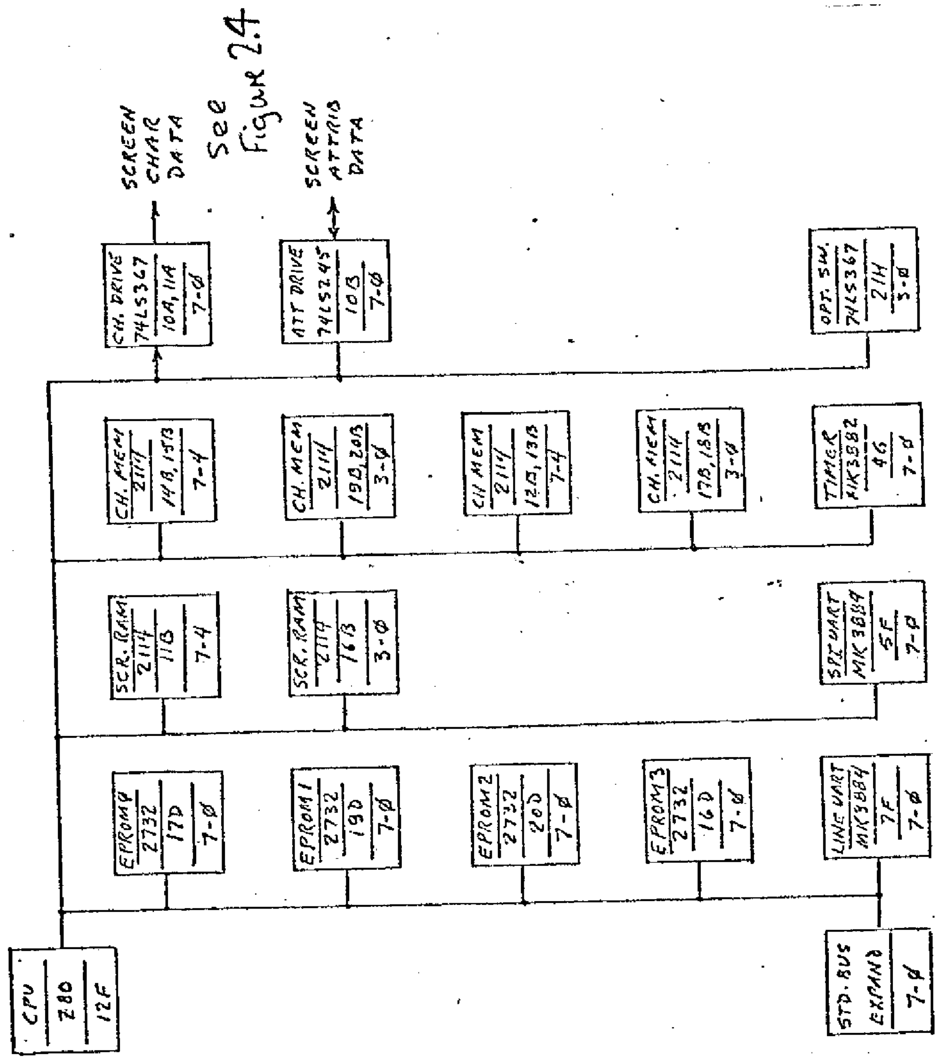


Figure 2.3 Block Diagram of the Data Bus

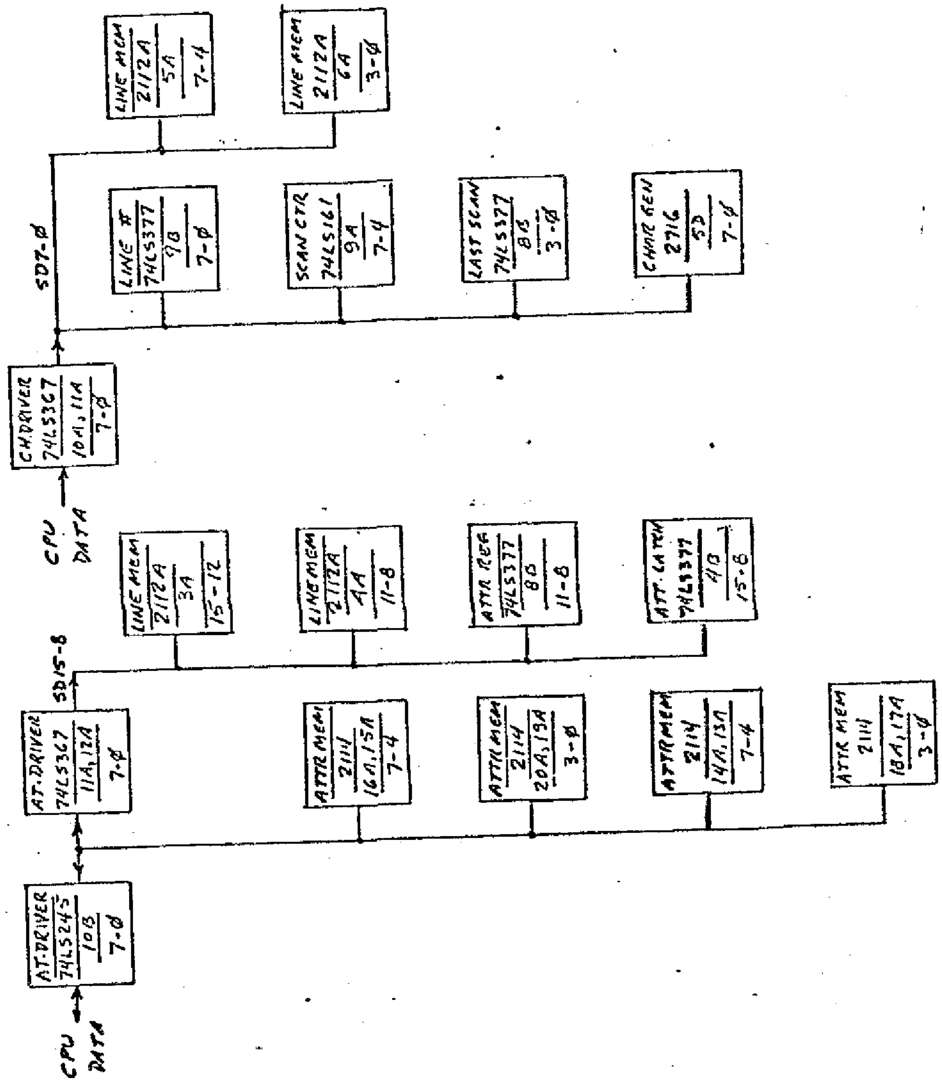


Figure 2.4 Block Diagram of the Screen Data Bus

The derivation and use of the signals are as follows:

a. RD (Read) signal is generated by the CPU to indicate that the CPU is in a read state, ready to read information from the host computer, keyboard, serial/parallel input port or signals from the timer. RD logically AND gated with MREQ (memory request) will produce MR (memory read) to tranfer the information is the program memory to the CPU.

b. MREQ (memory request) is generated by the CPU to indicate that the CPU requires informtion from the program memory. The address of the specific information will also be on the address bus so that when the memory read signal is generated, the program memory will transfer the information to the CPU.

c. WR (write) is generated by the CPU to advise the memory that the CPU is placing information on the data bus. This information will be written into the random access memory (RAM) module which has been addressed on the address bus.

d. IOREQ (I/O request) is generated by the CPU to indicate that the CPU is performing an input/output operation from the line UART, the SPI UART, or the timer circuit.

e. The M1 (memory cycle 1) signal, generated by the CPU is used by the I/O dervies to transfer information. The signal informs the I/O dervices that their interrupt request has been accepted.

f. The BUSAK (bus acknowledge) signal is generated by the CPU when it has finished an operation and has released control of the address and data buses. The address and data buses will then be available to any other device. Normally a CRT write signal will be used as a result of the BUSAK signal to start the first scan on the CRT screen.

g. The WAITRQ (wait request) signal is generated by the CPU, it is a scheduling signal to suspend read or write operations between the memories and the CPU. Normally memory access times are fast enough to ensure that WAITRQ cycles are not required. Although this signal is connected to the line UART and the SPI UART modules, it is not used by them.

h. The BUSRQ (bus request) signal generated by the CRT controller when it wants to start a CRT write cycle. The signal causes the CPU to suspend operations after the completion of the current instruction and thereby release control of the address and data buses.

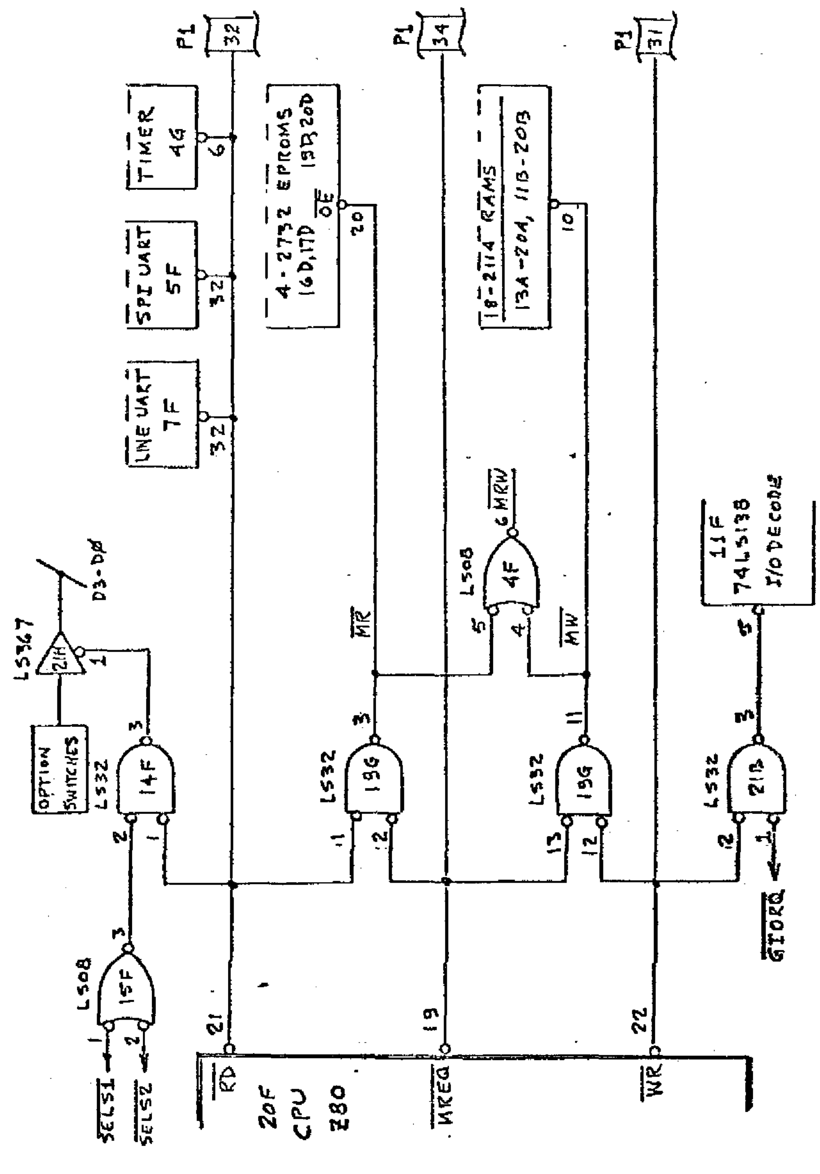


Figure 2.5 Block Diagram of the RD, MREQ and WR Signals

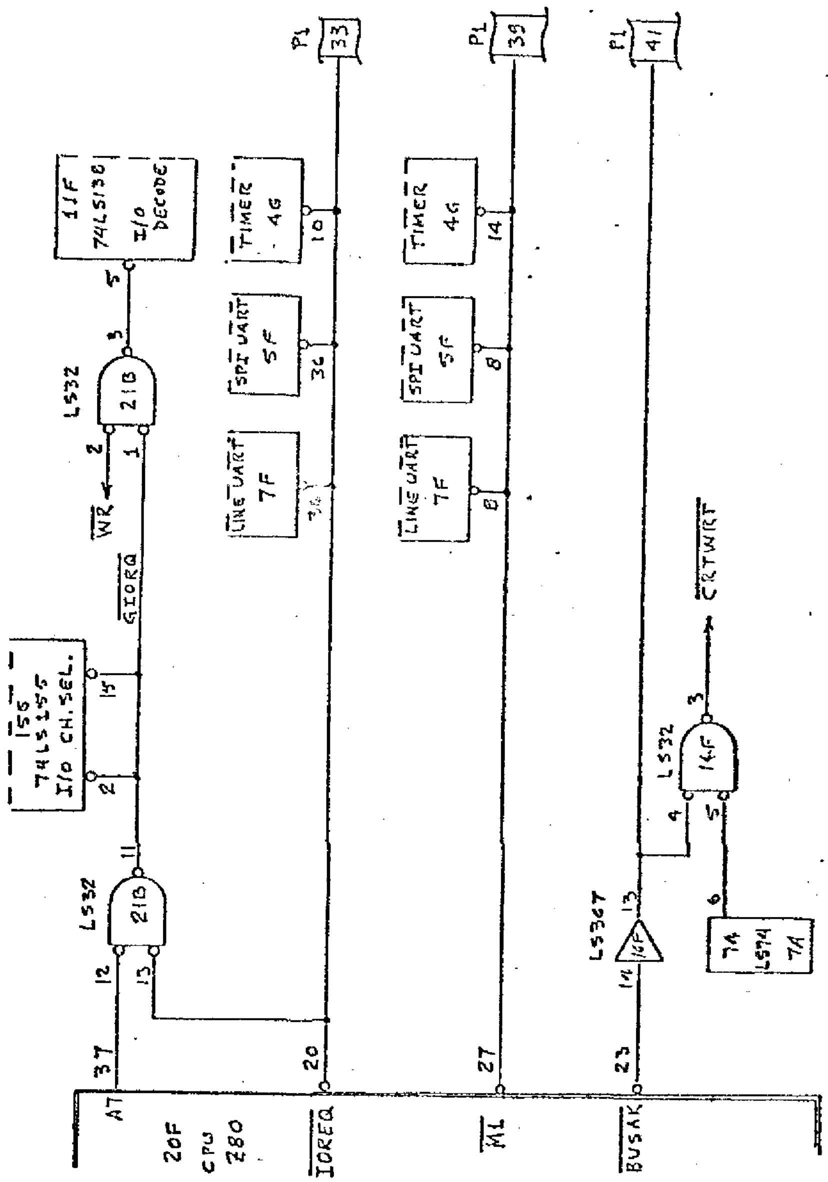


Figure 2.6 Block Diagram of the 1OREQ, M1, and BUSAK Signals

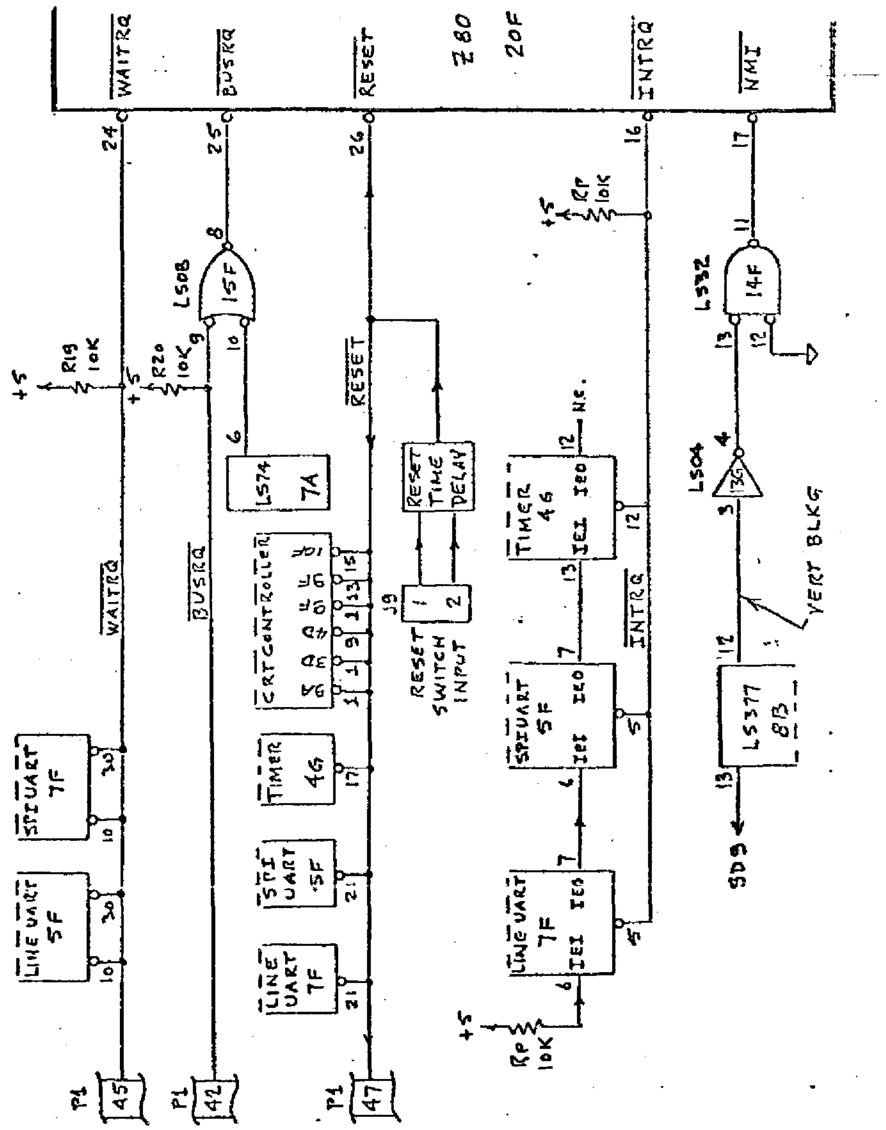


Figure 2.7 Block Diagram of the WAITRQ, BUSRQ, RESET, INTRO, and NMI Signals

i. The RESET signal resets the CPU, the UART's, the TIMER, and the CRT controller to their initial state. This signal is generated from the reset switch and is an external signal.

j. The INTRQ (interrupt request) signal is generated by the line UART, the SPI UART or timer indicating that they require the CPU to perform a specific instruction. The CPU completes its current instruction and jumps to read the data at the address given during the interrupt cycle. There is a priority order between the three sources as shown below:

Priority 1 line UART
Priority 2 SPI UART
Priority 3 TIMER

k. The NMI (non maskable interrupt) is a signal generated by the CRT controller to signify the beginning of the CRT vertical retrace interval.

2.2.4 Chip Select Bus

The chip select bus (CS bus) is part of the addressing function for the memory address. Logical combinations of address bits generate chip select signals to access particular memory addresses. This method of addressing reduces the number of connecting lines and the number of driver modules.

2.3 CRT CONTROLLER

The CRT controller schedules the information for display on the CRT screen. It breaks each character line into 10 scan lines, it also controls refresh timing to ensure that the characters stay visible on the CRT screen for the period of time required by the operator.

The CRT controller initiates an information write cycle by generating the signal CRTWRT (CRT write). This signal enables the CRT controller to access the CRT address and data drivers, and to place the address bus under the control of the CRT controller. The contents of the data bus is then available for transfer into the line buffer memory. CRTWRT also transfers the contents of the character and attribute memories into the line buffer memory forming a 12 bit wide data path containing the character, its position on the CRT screen, and its attribute.

2.3.1 Screen Data Bus

The inforamation conveyed on the screen data bus has to take into account a number of conditions. The first condition is that there are 10 scan lines to each character line, and that the complete line is scanned. The next condition is that attributes must be applied at the time the character or characters are built up on the screen. The third condition is that a blanking pulse must be generated at the end of each scan line to prevent the flyback trace from being visible on the CRT screen.

During the first scan of each character row the following events occur to achieve the above conditions:

a. The CRT controller activates the bus request signal to suspend operation of the CPU and to release the CPU from the address and data buses.

b. The CRT controller takes control of the address lines using the screen address drivers (location 12D, 13D, AND 15D on the controller PCB) to place the memory addresses generated by the controller, onto the screen data bus.

c. The screen character and attribute memory modules are addressed as a 4K by 12 bit wide memory whose output is copied (using the drivers located at 10A - 12A on the controller PCB) to the line buffer memory (located at 4A - 6A on the controller PCB).

d. Simultaneously to event c, the screen character data is copied into the character generator module (located at 5D on the controller PCB) to display the characters as they are copied; attribute data is copied to the attribute latch (located at 4B on the controller PCB) sending attribute information to the video circuits.

e. The first two data bytes read out of screen memory contain the information needed to operate the CRT controller; the next 80 bytes are character information. The CRT controller information required is:

- single or double-width characters
- vertical drive
- vertical blanking
- first scan count
- last scan count
- line number

2.3.2 Scan Counting

The screen scan rate is a function of time and to obtain a complete character line complete with any attributes, the CRT controller must be able to access screen memory exclusively. The CRT controller uses a DMA (direct memory access) operation to copy the memory contents into the four bit register, for the addresses of data for transfer to the drive circuits of the CRT.

There are two four bit registers (U8B on the controller PCB) loaded from the screen memory, the Last Scan No. Register, and the line Attribute Latch. The Last Scan No. Register contains the number of the last horizontal scan in the current character row. The contents of this register is fed to the Scan Count Comparator (U8A on the controller PCB) where it is compared for equality to the contents of the current Scan Counter (U9A on the controller PCB). The Scan Counter is loaded during the start of a DMA operation with the number of the first horizontal scan of the current character row. This counter is incremented as each horizontal scan of the character row is displayed. When the contents of the counter equals the output of the Last Scan No. Register, the Scan Count Comparator sends a signal to the First Scan Latch to indicate that the current character row is complete and the CRT controller then finishes the DMA copy operation allowing access to the screen memory.

The operation waits on an instruction to commence the DMA cycle for the next character row.

The Line Attribute Latch contains the addresses of the attributes affecting the entire character row.

2.3.3 Character Counting

During each horizontal scan a character position counter is incremented with the address of the character an its attribute to place each character in its correct format and position on the CRT screen.

The Character Line No. Latch (U9B on the controller PCB) is an 8 - bit register, which is also loaded during the CRT Controller DMA operations, contains the current character row number being displayed. The character row number is used by the Address Compressor (UIOD on the Controller PCB) to generate the screen memory addresses for which the character row will be assembled for display on the CRT. The most significant two bits of the Character Line No. Latch determine which pair of screen memory pages will be used for display.

The character row number is incremented by the Character Counter and the Character Counter Latch (UTB and U9d on th controller PCB) by forming a "state machine" supplying a binary count for the 80 displayed characters, the horizontal blanking signal, and the link-list addresssing sequence.

The timing of counters and registers loaded during the CRT controller DMA operations are clocked at the edge of the horizontal blanking signal. The horizontal blanking signal is delayed through the Line Attribute Timing Latch (U60 on the controller PCB) to cause clocking to occur at the correct time.

2.3.4 Blanking and Drive

The Horizontal Drive Logic (U14F, U15F, and U21B on the controller PCB), the Double Width Logic (U4F and U13F on the controller PCB), and the Line Attribute timing Latch combine the vertical blanking, the decoded character counter states, the double width, and the horizontal blanking to provide monitor drive signals.

2.4 DESCRIPTION OF LOGIC SCHEMATIC DIAGRAMS

This section is a short description of the function and identification of logical circuits in the logic schematic diagrams shown in Appendix A. This description will enable a technician to identify the function of a particular area on the schematic diagrams. The description is related to the sheet number in the title block of each sheet.

2.4.1 Schematic, 3100 Logic, Sheet 1

This sheet contains the CPU, its associated logic and the screen address drivers. The following major signals are generated on this sheet:

a. Bus Request (BUSRQ)
The BUSRQ signal is produced from the OR gate (15F) which allows bus requests either from the CRT controller or from the expansion connector.

b. RESET
The RESET signal is generated automatically on power-up, or from the expansion connector. The time duration of the signal is determined by the hysterisis feedback level restorer circuit consisting of R21, C80, and inverters BG and 12F.

c. Non-Maskable Interrupt (NMI)
The non-maskable interrupt signal, is generated by the CRT controller during each vertical retrace time. For test purposes this interrupt can be disabled by removing the ground connection at 14F pin 12.

2.4.2 Schematic, 3100 Logic, Sheet 2

This sheet contains the memory chip selection generating circuits, the EPROM memory, the scratch pad memory, and the screen chip selection combining circuit. The CRT controller reads character and attribute data from memory as a 12 - bit word. Screen character data is addressed from 8000 to 8FFF (hexidecimal), and attribute data from 9000 to 9FFF (hexidecimal). The CRT controller can only address the 8000 series addresses and uses the combining circuit to address the attributes concurrently with screen characters.

2.4.3 Schematic, 3100 Logic, Sheet 3

This sheet contains the screen memory and memory data I/O circuits. The 12 - bit data word for the CRT line buffer memory are derived from drivers 10A, 11A, and 12A, during CRT write time.

2.4.4 Schematic, 3100 Logic, Sheet 4

This sheet contains the counter timer, the clock pulse oscillator, the clock pulse divider, the bell control, and the keyboard and bell clock pulses.

a. The counter timer (4G) generates the three UART clocks and a programmable interrupt time delay. It consists of four independant timers programmed form the CPU. The three UART clock timers use the system clock pulse to provide clock outputs at pins 7, 8, 9. The software timer uses a longer frequency clock input on pin 20 to generate longer time delays. The software timer can interrupt the CPU using the INTRQ signal assuming the interrupt priority enable (IEI) is a logical one. The UART clocks run continuously.

b. The clock pulse oscillator generates the master clock of 14.7456 MHz.

c. The clock pulse divider generates the CPU system clock of 14.7456 MHz or 2.4576 MHz using modules 4F, 12F, 2F, and 2G.

d. The bell control is controlled by the I/O commands IO7 (bell on) and IO8 (bell off), from modules 2G and 13F.

e. Keyboard and bell clock pulses are generated by 1G an 1F using the system clock pulse as input. The keyboard clock is 30.72 KHz, the bell clock is 1920 Hz, and the timer clock is 960 Hz.

2.4.4 Schematic, 3100 Logic, Sheet 5

This sheet contains the connections to the UART's the level converters, the line output and the optional SPI port output lines.

2.4.5 Schematic, 3100 Logic, Sheet 6

This sheet contains all the set-up and option switch circuits. Decoders 14H, 16H, 19H and 20 H are 3 - to - 8 decoder modules to select switch sections under the control of address lines A0 and A1 using the enable signals CSSW1 or CSSW2. Four switch sections are read in parallel at any one time and the result connected to the CPU address bits 0 and 3.

2.4.6 Schematic, 3100 Logic, Sheet 7

This sheet contains the scan counting and part of the character counting circuits.

2.4.7 Schematic, 3100 Logic, Sheet 8

This sheet contains the remainder of the character counting circuit, and the blanking and drive circuits.

2.4.8 Schematic, 3100 Logic, Sheet 9

This sheet contains the video output circuits. The video is set to one of four levels (off, dim, normal, bright) dependant on the value of the attribute bits and the character selected. The screen background can be either black (off) or white (on).

The module IC retimes the two video channels to eliminate spurious timing dots caused by propagation delays through the attribute logic.

The ratio of the four video levels is set by the value of resistors R7, R10, R11, and R12. The amplitude is set by the values of resistors R8 and R13.

Transistor Q2 is an emitter follower providing a variable-voltage DC source to drive the video output ciruits. The contrast control on the front panel determines the amplitude of the video output by setting the DC voltage level at the base of Q2. Resistor R5 sets the maximum voltage available for the video output, and thus the maximum contrast available.

2.5 KEYBOARD

The keyboard contains the operator controls of the NABU 3100 terminal. The layout of the keys is in a standard QWERTY form with an extra set of function keys as a top layer. A separate key pad is located to the right of the keyboard. Some keys are multi-function as defined in the NABU 3100 Users Manual.

The keyboard contains a micro-processor to read the key pads, format the output coding, and perform control functions.

2.5.1 Keyboard Microprocessor

The keyboard microprocessor contains an integral read only memory (ROM) with a pre-determined program written into the memory. This program interprets the key position and designates a code for it, this code is output from the microprocessor as a number of bytes of data (dependant on the character or function selected on the keyboard). The program in the microprocessor cannot be altered by the operator. The operations performed by the microprocessor are timed by an external crystal oscillator running at 6MHz.

2.5.2 Key Matrix Scanning

The microprocessor outputs a binary count on its output ports P20 through P23 to the two decoder modules, and reads the input ports P11 through P17. When a key is operated, the binary count is altered and the signal to the input port is altered. The program in the microprocessor identifies these changes and relates them to a code representing the character code. The microprocessor scans the keyboard at a rate proportional to the oscillator and outputs the character code as soon as a change in the matrix is detected.

2.5.3 Keyboard Output

When a key is operated, a two or three byte transmission of data will occur. These bytes wil be status and data as shown in Figure 2.5. Diodes are connected to the ends of the matrix to prevent phanton output characters.

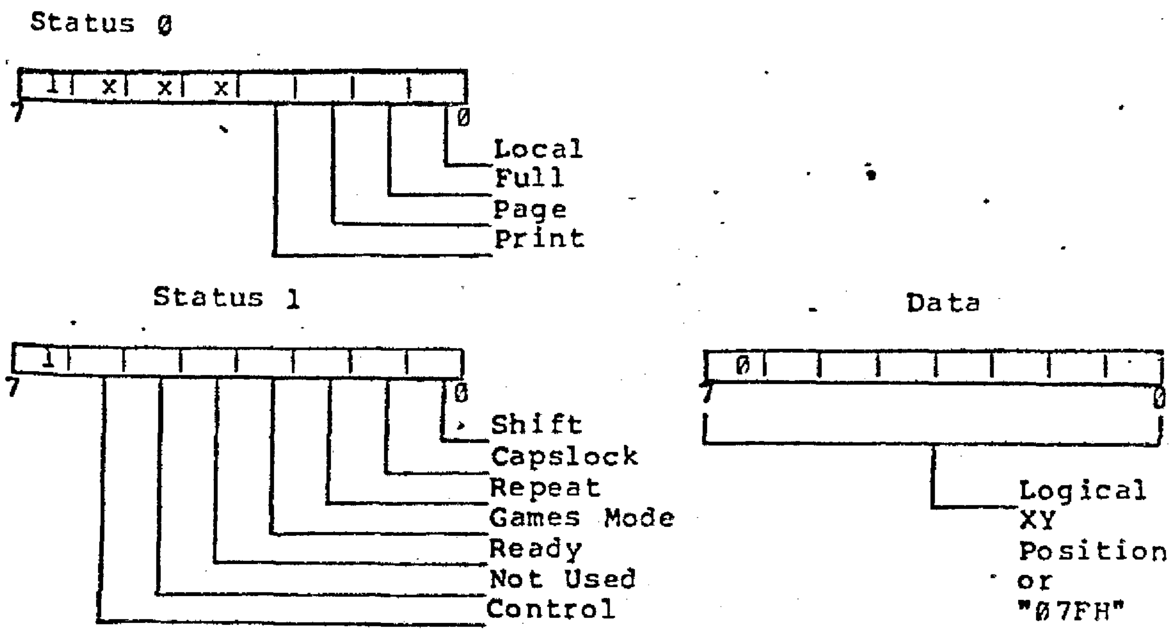


Figure 2.5 **Format of Output Characters**

CHAPTER THREE

TROUBLESHOOTING AND REPAIR

CHAPTER THREE - TROUBLESHOOTING AND REPAIR

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3.1 GENERAL

This chapter establishes techniques for testing and troubleshooting the NABU 3100. It is important to define the problem area and to apply a logical procedure to isolate the faulty component or components.

3.2 TROUBLESHOOTING PROCEDURES

When troubleshooting the NABU 3100 it is an advantage to carry out a set of procedures in a sequential method to recognize the problem and to locate the faulty component. The procedure contains task outlines each with an alphabetical prefix. Group A task outline is the primary sequence which will identify the problem area and direct the technician to the next group task outline. For any problem it is advisable to start with Group A because it will also identify problem areas for multi-fault situations, for this reason goup A is called Initial Check.

3.2.1 Initial Check, Group A

The initial check of the NABU 3100 is listed sequentially in Table 3.1.

STEP	SYMPTOM	POSSIBLE FAULT	ACTION
A1	No operation	incorrect installation	Check security of connector. Check that power card is connected to correct power source. Check that front panel controls are effective.
		Dip switch setting incorrect	Adjust DIP switches according to User Manual.
A2	No short "beep" (1 second) when switching on.	Power supply failure	Go to 3.2.2
A3	The "beep" is of 2 second duration when switching on.	Logic board fault	Go to 3.2.5
A4	No lights on screen (scan lines, Characters, nonesense data etc.)	Fault in monitor circuit	Go to 3.2.3
A5	A single vertical or horizontal line on the screen	Fault in monitor circuit	Go to 3.2.3
A6	Information on the screen is rolling (vertically or horizontally)	Fault in monitor circuit	Go to 3.2.3

Table 3.1 Initial Check, Group A

STEP	SYMPTOM	POSSIBLE FAULT	ACTION
A7	Incorrect display appears when pressing "SET UP" key on keyboard	No response at all (keyboard fault) Incorrect characters (logic fault)	Go to 3.2.4 Go to 3.2.5
A8	With unit in LOCAL mode, incorrect characters on screen	If occassionally missing characters the keyboard is faulty A group of characters missing indicates a logic fault	Go to 3.2.4 Go to 3.2.5
A9*	In REMOTE mode, transmit and receive data is missing or incorrect	Logic fault	Go to 3.2.5

* For this step a test configuration must be used. The terminal under test must be configured as follows:

a. The unit must be in REMOTE mode using SETUP mode or selected at the DIP switches.

b. A known good terminal must be connected to the unit under test through the main serial I/O port.

c. Transmit data pin 2 should connect to input pin 3 of good terminal. Receive data pin 3 should connect to output pin 2 of good terminal, and ground pin 7 should connect to ground pin 7 of good terminal.

d. The baud rates should be the same on both terminals.

Table 3.1 **Initial Check, Group A (continued)**

3.2.2 Power Supply, Group B

A DC voltmeter and an AC voltmeter of suitable range are used to verify the operation of the power supply. Instead of separate meters a multimeter is acceptable as a test instrument. Table 4.2 lists the steps in sequential order.

STEP	TEST	POSSIBLE FAULT	ACTION
B1	The DC voltages are checked at J8 on the Controller PCB +12v (pin 1) voltage check	If +12 v is not within 5% of nominal, VR2 and associated circuit components are faulty.	Change VR 2,* and or the associated diodes and Capacitors
	+5V (pin 2, nominal V is 5.15) voltage check	If the voltage is not within 5% of 5.15V, the +5V voltage regulator is faulty	Adjust R25 or change VR3*
	+5V (pin 4) voltage check	If the +5V is not within 5% of 5.00V the +5V voltage regulator is faulty	Adjust R24 or change VR1*
	-12V (pin 5) voltage check	If the -12V is not within 5%, the reference voltage regulator is faulty	Change VR1 on Controller PCB

Table 3.2 **Power Supply, Group B**

STEP	TEST	POSSIBLE FAULT	ACTION
B2	The AC voltages are checked at J11 on the controller PCB. 8V (pins 1 & 2) voltage check	If 8V is not within 25% of nominal, the transformer T1 is faulty	Change the transformer, T1
	13V (pins 3 & 4) voltage check	If 13V is not within 25% of nominal, the transformer T1 is faulty	Change the transformer, T1
	All voltages 50% or more out of tolerance	Primary wiring incorrect	Check wiring and source voltage. Rectify where necessary
B3	No voltages at any of the secondary windings of transformer T1	Fuses faulty, line filter open circuit, power switch or primary wiring faulty	Using the schematic diagrams verify that the items of the power input, function correctly. Replace where necessary.

* On regulator heatsink assembly bolted to chassis.

Table 3.2 **Power Supply, Group B (continued)**

3.2.3 Primary Check of Monitor, Group C

There are a number of simple checks that can be carried out to verify the condition of the Monitor circuit. The checks consider the SAMSUNG Monitor only. The information for the MON-4 Monitor is contained in Appendix B. If the Monitor is found faulty, it may be further tested by using the information in 3.3. The primary check of the monitor is listed sequentially in Table 3.3.

STEP	TEST	POSSIBLE FAULT	ACTION
C1	Using a DC voltmeter connected to pins 10 and 7 of the edge connector, verify that the voltage is within tolerance	If the voltage is not within 11 and 13V the wiring and/or power supply is faulty	With the aid of the schematic diagrams check the power supply and wiring. Rectify as necessary.
C2	Using a suitable oscilloscope at J4 (pin 2) on the controller PCB, verify that the wave form of the vertical drive is within tolerance	If the waveform of the vertical driver is not in accordance with Figure 3.1, the drive circuit is faulty.	With the aid of the schematic diagrams check vertical driver amplifier and driver. Rectify as necessary
	Using a suitable oscilloscope at J4 pin 4 on the controller PCB, verify that the ripple on the +12V supply is less than 200mV	If the ripple is excessive the +12V power supply is faulty	With the aid of the schematic diagrams check the operation of the +12 power supply. Rectify as necessary.

Table 3.3 **Primary Check of Monitor, Group C**

STEP	TEST	POSSIBLE FAULT	ACTION
C3	After adjusting the brightness control to obtain a rectangle of scan lines, verify that there is data or a cursor line	If there is nothing on the screen the Video circuit in the monitor is faulty	Refer to 3.3 to troubleshoot the monitor
	Horizontal line only on display	Vertical circuit in monitor faulty	Refer to 3.3 to troubleshoot the monitor
	Vertical line only on display	Horizontal circuit in monitor faulty	Refer to 3.3 to troubleshoot the monitor.

Table 3.3 **Primary Check of Monitor, Group C (continued)**

3.2.4 Keyboard, Group D

The keyboard is tested when connected to the terminal. All supply voltages for the keyboard are derived from the terminal display unit. The keyboard checks are listed sequentially in table 3.4.

STEP	SYMPTOM	POSSIBLE FAULT	ACTION
D1	Malfunction of the keyboard, identified from Initial Check, Group A.	No output from the keyboard.	Connect oscilloscope or logic probe to J3 pin 2 on controller logic PCB. Verify that there are pulses on this pin when various keys are operated on the keyboard. If there are no pulses on the pin go to step D5.
D2		Incorrect voltage levels in the keyboard	Measure the keyboard power at Z1 between pins 16 and 8 (put positive lead on pin 16), the voltage should be between 4.75 and 5.25V dc. If there is no voltage check the keyboard cable and or power supply in the controller logic PCB. If the voltage is out of tolerance check the voltage at J3 pin 1, adjust R25 to obtain 5.15V.

Table 3.4 **Keyboard, Group D**

STEP	SYMPTOM	POSSIBLE FAULT	ACTION
D3		Faulty keyboard cable	Connect the oscilloscope or logic probe to U5 pin 35 on the keyboard. If there are pulses present when keys are operated, the keyboard cable is faulty and should be changed. If there are no pulses go to step D4.
D4	No output from micro processor	Faulty crystal Y1 Faulty micro processor Z4	Connect the oscilloscope or logic probe to Z1 pin 13 and verify that there is a square wave output. If not, change the crystal Y1 and or microprocessor Z4, if necessary.
D5	Single keyswitch malfunctioning	High resistant contacts	Replace contacts
D6	Group of keyswitches malfunctioning	Decodes integrated circuits faulty.	Check the keyswitch decoders and replace if necessary.

Table 3.4 **Keyboard, Group D (continued)**

3.2.5 Controller Logic

When it has been established that the controller logic is faulty (from Group A), use an oscilloscope in conjunction with the schematic diagrams in Appendix A to identify and rectify the fault.

3.3 DETAILED TROUBLESHOOTING OF MONITOR

The monitor in the NABU 3100 is the SAMSUNG unit, the troubleshooting techniques are for this monitor. If the faulty NABU 3100 contains the MON-4 monitor refer to Appendix B for details. Table 3.5 contains troubleshooting procedures for the SAMSUNG monitor.

SYMPTOM	POSSIBLE FAULT	ACTION
No Raster	Brightness control not adjusted properly.	Turn brightness control R510 clockwise to maximum. If problem still persists proceed to next step.
	CRT heater is not functioning.	Check CRT, heater voltage, power supply circuit and CRT socket for normality. If problem still persists proceed to next step.

Table 3.5 **Troubleshooting Chart for the Monitor**

SYMPTOM	POSSIBLE FAULT	ACTION
	High voltage not obtainable.	Check flyback transformer, T402. Check collector pulse of Q404. Check base pulse of Q404. Check collector and base waveforms of Q403. Check input HD. If all measurements are correct proceed to next step; if not, replace faulty components. G2: 350V to 450V G4: -100V to 400V G1: -100V to 20V K: 0 to 50V
	No voltage at G2 and G4.	Check CR501, C501, R501, R505, R507, R503, R508, R509 and T402.
	No voltage at G1.	Check CR502, CR503, R502, R510, R511, R506, C503, C504, E502, and T402.
	No voltage at K.	Check CR502, R204, R206, E501, and T402. Replace any components in check list found to be faulty.
No Raster (Cont.)	Voltages of G2, G4, G1 and K are normal.	Replace faulty CRT.

Table 3.5 **Troubleshooting Chart for the Monitor (Continued)**

SYMPTOM	POSSIBLE FAULT	ACTION
Only one raster line appears in horizontal direction.	Deflection yoke vertical coil is not 30-50 ohms.	Replace.
Only one raster line appears in vertical direction.	Wire breakdown, defective yoke horizontal coil, or L402, L403, or C413 open.	Replace.
Deformed raster.	Shorting of deflection yoke coil.	Replace entire deflection yoke.
Abnormal raster movement or excessive picture fluctuation.	Abnormal power supply, current surges or alternating magnetic field near unit.	Check and measure that the ripples of power supply are less than 10mV p-p. If ripples are normal, check for intruding magnetic source.
Spot remains when power turned off.	Defective components.	Check C502, C503, and CRT for deterioration. Replace when necessary.
Brightness range is abnormal.	Deterioration of CR503, C503, or CRT.	Check voltage of G2 heater, Q201, E501, R503 R204, R205, CR502, and C502. Replace defective components when necessary.
Raster size is too small and picture is too bright.	High voltage is abnormally high.	Check C409, C410, and T402. Replace defective components.

Table 3.5 **Troubleshooting Chart for the Monitor (Continued)**

SYMPTOM	POSSIBLE FAULT	ACTION
No vertical synchronization.	Vertical deviation is abnormal.	Check VD, C301, R302, and U301. Adjust VD and if, problem persists, replace defective components.
Deviated raster position.	Magnet needs centering.	Turn deflection yoke, centering magnet so that raster is positioned at center.
Picture or characters do not appear; no contrast achievable.	Faulty components or CRT.	Check Q201 and associated components. Check video input signal. Check CRT.
Inclined picture and/or characters.	Yoke out of adjustment.	Loosen clamp screw on deflection yoke. Rectify the inclination by turning the entire deflection yoke.
Picture noise or characters 'shiver'.	Voltage leaks or component non-contact.	Check high-voltage portion for leakage. Check connectors for complete contact.
Picture takes too long to appear. (>15 sec.)	Service life of CRT has been exceeded.	Replace CRT.

Table 3.5 Troubleshooting Chart for the Monitor (Continued)

SYMPTOM	POSSIBLE FAULT	ACTION
Sync noise.	Poor electrical contact.	Check grounding wire for poor contact. Check video ground wire and power supply wire for incompleteness. Check input signal for normality. Replace defective parts where required.
Picture appears and disappears alternately.	Poor electrical contact.	Check input signal. Check card edge connector. Check video circuit for poor soldering. Check CRT socket.
No horizontal linearity.	Faulty components.	Check L403, C413, and Q404. Replace defective components where necessary.
No vertical linearity.	Faulty components.	Check R306, R307, C304, C305 and U301. Replace defective components where necessary.
Focusing is not achievable.	Components require adjustment, incorrect voltage, or faulty CRT.	Check voltages of G2 and G4. Readjustment of R508. Check high-voltage. Check CR501, R501, C501, R503, and R509. When all above items check out as normal, CRT is faulty and should be replaced.

Table 3.5 **Troubleshooting Chart for the Monitor (Continued)**

CHAPTER FOUR

DISASSEMBLE AND REPAIR

CHAPTER FOUR - DISASSEMBLE AND REPAIR

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WARNING

The voltages used in this equipment are sufficiently high to endanger human life. Every reasonable precaution has been observed in design to safeguard the operating personnel. The power should be removed completely, and high voltage capacitors should be discharged in accordance with the instructions printed on the labels adjacent to the source of the high voltage, using a shorting bar, before carrying out any repair or disassembly.

To prevent excessive x-ray emissions from the cathode ray tube, do not exceed the rated high tension voltage.

4.1 DISASSEMBLY

4.1.1 Keyboard

There are no special disassembly or assembly instructions required for the keyboard. The following notes are offered as an aid:

1. To remove the keyboard surround, use a wooden pry blade to release the top from the housing. Protect keys, particularly the **SEND ENTER** key, when removing the keyboard surround.

2. The keyboard-display interface cable can only be removed after the keyboard surround is removed.

3. Keys are mounted in function blocks. (Refer to Chapter 7 for unit blocks).

4. Assembly is the reverse of disassembly.

4.1.2 Display

There are no special disassembly or assembly instructions required for the display. The following notes are offered as an aid:

1. With the power cord removed, remove two screws at the rear of the cover, partially remove the cover, remove the ground wire and then totally remove the cover.

2. Discharge the high tension (HT) voltage in accordance with the warning label on the cathode ray tube (CRT).

3. Removal of the printed circuit boards is straightforward.

4. Do not remove the yoke from the CRT unless absolutely necessary.

5. Removal of the CRT complete with yoke is straightforward.

4.2 REPAIR

CAUTION

Use a low voltage, low wattage soldering iron to effect repairs on printed circuit boards. Ensure that the soldering iron is correctly grounded before use.

4.2.1 General

When replacing integrated circuits (ICs) or transistors that are soldered onto the printed circuit board (PCB), observe the following procedures:

1. Using diagonal cutters, cut the connections of the faulty component and discard.

2. Remove the remaining connections on the PCB using a soldering iron and tweezers. Do not use excessive heat.

3. Use a solder remover to clear the component mounting holes.

4. Preform the wire connections on the components prior to positioning on the PCB.

5. During the soldering phase, protect the components using suitable heat sinks.

6. Inspect the PCB after soldering for excess solder and shorting of track; rectify if necessary.

7. Clean excessive flux from the PCB using a suitable solvent.

8. Carry out a functional check of the system, after each component change, to verify the results.

4.2.2 Keyboard

There are no specific repair procedures for the keyboard. The following notes are offered as an aid:

1. When replacing keysets, do not overheat the PCB, and use a solder remover to assist in removing keysets.

2. To remove key tops, pry with fingers only.

3. Damaged PCBs should be replaced; no attempt should be made to repair damaged track.

4.2.3 Display Unit

There are no specific repair procedures for the display unit. The following notes are offered as an aid:

1. It is recommended that the CRT and yoke be changed as a set. If either of the components are changed, a complete check of the orientation of the CRT display must be carried out.

2. Damaged PCBs should be replaced; no attempt should be made to repair damaged track.

CHAPTER FIVE

ALIGNMENTS

CHAPTER SIX

SERVICE PARTS LIST

CHAPTER SIX - SERVICE PARTS LIST

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6.1 INTRODUCTION

The majority of the components used in the NABU 3100 are industry standard parts easily obtainable through local sources. The items that are unusual or manufactured by NABU Manufacturing Corporation are identified in this chapter.

6.2 KEYBOARD

Table 6.1 contains the items for the keyboard that are available through NABU Manufacturing Corporation, alternate sources are also identified.

Description	Part Number	Alternate Source
PCB Assy. with space bar less keytops	75-250-00007-3	
PCB Assy. with spacebar less keytops and microprocessor	(old) 74-250-00007-5 (new) 74-250-00009-1	Interchangeable with (new) Hi-Tek
Micro processor - 8748 (programmed)	59-000-00365-3 or 59-000-00478-4	
Plunger - Momentary	15-000-00002-5	Hi-tek 173-40213
Plunger - Locking	15-000-00009-6	Hi-tek 173-40334
Cam-locking	15-000-00010-4	Hi-tek 173-40260
Spring - 2 oz	15-000-00004-1	Hi-tek
Contact-Solid	15-000-00000-9	Hi-tek 173-30107
Contact-Fingered	15-000-00001-2	Hi-tek 173-30108
Tool for Contact replacement	97-000-00000-7	Hi-tek 173-10023
Cable - coiled	24-000-00003-9	BERG 66466-011

Table 6.1 **Service Parts List For The Keyboard**

6.3 CONTROLLER

The controller users standard integrated circuits which have their vendor identification number printed on the top. Custom produced items for the controller are listed in Table 6.2.

Description	Part Number	Alternate Source
PCB Assy. (old) (new)	71-250-00002-6 71-250-00023-9	
Crystal 14.7456 MHz	81-000-00001-3	Midland Ross HC-18/U
Transducer	27-000-00000-4	CGE SSH-01 AHP
EPROM U5D	59-000-xxxxx-x (x programmed on label)	
EPROM U9D (programmed)	59-000-00412-6	
PROM U10D (programmed)	59-000-00413-9	
EPROMS U16D, U17D, U19D, U20D (Programmed xxxxx-x on label)	59-000-xxxxx-x	
Transformer Assy	74-000-00035-5	
Transformer Only	29-000-00000-0	
Keyboard Connector Assy	74-250-00004-6	

Table 6.2 **Service Parts List For The Controller**

Description	Part Number	Alternate Source
Keyboard Connector Only	52-000-00001-4	BERG 65903-008
Contrast Control Assy	74-000-00008-9	
Contrast Control Only	57-000-00000-1	

Table 6.2 Service Parts List For The Controller (continued)

6.4 MONITOR

The monitor assembly is one of two types, SAMSUNG or MON-4 identifable by the part number on the PCB assembly. Custom produced items for the monitor are listed in Tables 6.3 and 6.4.

Description	Part Number	Alternate Source
PCB Assy	74-000-00042-1	SAMSUNG 00-05-905
Flyback Transformer	29-000-00009-7	SAMSUNG 542-03-001
Horizontal Output Transistor	84-100-53407-9	SGS ATES BU407D
Vertical Processor IC	59-000-000483-4	SGS ATES TDA1170S
Yoke Assy	74-000-00043-4	SAMSUNG 000-01-007
CRT - White - Green - Amber	30-000-00012-8 30-000-00013-1 30-000-00014-4	SAMSUNG 12ZBY4 SAMSUNG 12ZBY31 SAMSUNG 12ZBYLA

Table 6.3 **Service Parts List For The SAMSUNG Monitor**

Description	Part Number	Alternate Source
PCB Assy	71-250-00031-8	
Flyback Transformer	29-250-00001-2	TOTOKU TMF108
Width Coil	29-040-40301-0	
Yoke Assy	74-000-00017-1	
Yoke Only	90-000-00002-7	TOTOKU TKD-2703
CRT - White - Green - Amber	30-904-12000-7 30-931-12000-3 30-900-23004-7	PHILIPS 12ST5470J (P4) PHILIPS 12ST5470P31J PHILIPS 12ST5470PLAJ

Table 6.4 Service Parts List For The MON-4 Monitor

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